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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,614	02/06/2004	John M. Brennan	2-81-1-4	7750

7590 11/20/2006

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EXAMINER	
KEBEDE, BROOK	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,614	BRENNAN ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *14-18 and 25* is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 18-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-7 and 9-13, and 18-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu et al. (US 2003/0122238) in view of Drake et al. (US 4,961,821).

Re claim 1, Wu et al. disclose a semiconductor device, comprising: an integrated circuit die (16), the integrated circuit die having at least one chamfer (i.e., the inclined portion on the four corners of the die 16) extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 2) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides (see Fig. 2, Page 2 Paragraph [0025]).

However, Wu et al. do not specifically disclose the chamfer being formed by an etching process.

Drake et al. disclose a semiconductor device, comprising: an integrated circuit die (see Figs. 9A-9E), the integrated circuit die having at least one chamfer (i.e., a groove 37 as shown in Fig. 9D) the chamfer being formed an etching process (see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

As Drake et al. disclose, the etch process utilized in order to form the beveled side wall on the IC die.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Wu et al. reference with an etching process as taught by Drake et al. in order to form the beveled side wall on the IC die.

Re claim 2, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the etching process consisting of at least one of wet etching and reactive ion etching (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 3, as applied claim 2 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the wet etching comprises anisotropic etching (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 4, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the at least a portion of the at least one perimeter edge of the integrated circuit die is beveled by forming one or more v-shaped

grooves in an upper surface of the device (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 5, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the at least one chamfer of the IC die is controlled, at least in part, by selectively varying one or more characteristics of the etching process (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 6, as applied claim 5 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the one or more characteristics of the etching process comprises at least one of a type of etchant, a temperature and a duration of etching (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 7, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including a plurality of integrated circuit die, at least one of the integrated circuit die being separated from the semiconductor device by: (i) forming one or more v-shaped grooves in an upper surface of the device, the v-shaped grooves defining perimeter edges of the at least one integrated circuit die;, and (ii) removing a back surface of the semiconductor device opposite the upper surface of the device until at least a portion of the v-grooves are exposed; wherein a sidewall of each of the v-shaped grooves forms a beveled perimeter edge of the separated die (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 9, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the IC comprises a plurality of

chamfers joining a respective pair of adjacent sides of IC die and having an upper surface which is angled relative to the respective pair of adjacent sides (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 10, as applied claim 9 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the respective angles of the upper surfaces of the chamfers relative to corresponding pairs of adjacent sides of the IC die are substantially matched to one another (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 11, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the at least one chamfer in the integrated circuit die is substantially matched to an angle of a sidewall of a die collet configurable for receiving the die (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 12, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein at least two perimeter edges of the integrated circuit die are beveled by the etching process (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 13, as applied claim 1 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein all perimeter edges of the integrated circuit die are beveled by the etching process (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 18, Wu et al. disclose a method for reducing post-fabrication surface damage to an integrated circuit die, the method comprising the step forming least one chamfer (see Fig. 2) in the at least IC die, the chamfer extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 2) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides (see Fig. 2, Page 2 Paragraph [0025]).

However, Wu et al. do not specifically disclose the chamfer being formed by an etching process.

Drake et al. disclose a semiconductor device, comprising: an integrated circuit die (see Figs. 9A-9E), the integrated circuit die having at least one chamfer (i.e., a groove 37 as shown in Fig. 9D) the chamfer being formed an etching process (see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

As Drake et al. disclose, the etch process utilized in order to form the beveled sidewall on the IC die.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Wu et al. reference with an etching process as taught by Drake et al. in order to form the beveled side wall on the IC die.

Re claim 19, as applied claim 18 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation the step of controlling an angle at which the at least a portion of the upper surface of the at least one chamfer by selectively varying one or more characteristics of the etching process (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 20, as applied claim 18 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the step of forming the at least chamfer comprises forming one or more v-shaped grooves in an upper surface of the integrated circuit (see Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 21, as applied claim 18 above, Wu et al. and Drake et al. in combination disclose all the claimed limitations including the limitation wherein the step of forming at least one chamfer comprises the step of substantially matching the angle of the upper surface of the chamfer to an angle of at least one sidewall of a die collet configurable for receiving the die (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 22, Wu et al. disclose a packaged integrated circuit device, comprising: at least one integrated circuit die, die having at least one chamfer (see Fig. 2) extending form a top surface of the integrated circuit to an intersection of first and second adjacent sides (see Fig. 2) of the IC die, the chamfer having upper surface which is angled relative to the first and second adjacent sides (see Fig. 2, Page 2 Paragraph [0025]).

However, Wu et al. do not specifically disclose the chamfer being formed by an etching process.

Drake et al. disclose a semiconductor device, comprising: an integrated circuit die (see Figs. 9A-9E), the integrated circuit die having at least one chamfer (i.e., a groove 37 as shown in Fig. 9D) the chamfer being formed an etching process (see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

As Drake et al. disclose, the etch process utilized in order to form the beveled sidewall on the IC die.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to provide Wu et al. reference with an etching process as taught by Drake et al. in order to form the beveled side wall on the IC die.

Re claim 23, as applied claim 22 above, Wu et al. and Drake et al. disclose all the claimed limitations including the limitation wherein the at least a portion of at least one perimeter edge of the at least one integrated circuit die is beveled by forming one or more v-shaped grooves in an upper surface of the at least one integrated circuit die (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Re claim 24, as applied claim 22 above, Wu et al. and Drake et al. disclose all the claimed limitations including the limitation wherein the angle of the upper surface of the chamfer in the at least one integrated circuit die is controlled, at least in part, by selectively varying one or more characteristics of the etching process (see Wu et al. Fig. 2, Page 2 Paragraph [0025]) and see Drake et al. Figs. 9A-9E, 10A-11B; and related text in Col. 4, line 49 – Col. 6, line 32).

Allowable Subject Matter

3. Claims 14-17 and 25 are allowed over prior art of record.

***Response* to Arguments**

4. Applicant's arguments with respect to claims 1-7 and 9-13, and 18-24 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. **THIS ACTION IS MADE NON-FINAL.**

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede
Primary Examiner
Art Unit 2823

BK
November 13, 2006